ZERO FORCING EQUALIZER DESIGN
FOR SIGNAL INTEGRITY APPLICATION

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ZERO FORCING EQUALIZER DESIGN
FOR SIGNAL INTEGRITY APPLICATION

by

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<table>
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<tr>
<td>ADS</td>
<td>Advanced Design System</td>
</tr>
<tr>
<td>BT-RTE</td>
<td>Block Transmission-Based Time-Reversed Equalization</td>
</tr>
<tr>
<td>CTLE</td>
<td>Continuous Time Linear Equalization</td>
</tr>
<tr>
<td>DFE</td>
<td>Decision Feedback Equalizer</td>
</tr>
<tr>
<td>DDR</td>
<td>Double data rate</td>
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<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ISI</td>
<td>Intersymbol Interference</td>
</tr>
<tr>
<td>LAN</td>
<td>Local Area Network</td>
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<tr>
<td>MIMO</td>
<td>Multiple-Input Multiple-Output</td>
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<tr>
<td>MLSE</td>
<td>Maximum Likelihood Sequence Estimate</td>
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<tr>
<td>MMSE</td>
<td>Minimum Mean-Squared Error</td>
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<td>OFDM</td>
<td>Orthogonal Frequency Digital Multiplexing</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>PCI Express</td>
<td>Peripheral Component Interconnect</td>
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<td>PRBS</td>
<td>Pseudo Random Bit Sequence</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>SATA I</td>
<td>Serial Advanced Technology Attachment I</td>
</tr>
<tr>
<td>SATA III</td>
<td>Serial Advanced Technology Attachment III</td>
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<td>TEM</td>
<td>Transverse Electromagnetic</td>
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<tr>
<td>Tx-FIR</td>
<td>Transmitter- Finite Impulse Response</td>
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<tr>
<td>USB 3.0</td>
<td>Universal Serial Bus 3.0</td>
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<tr>
<td>ZFE</td>
<td>Zero Forcing Equalizer</td>
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pesudo menunjukkan tahap ketepatan untuk pengiraan memaksa sifar samada berjaya atau tidak. Melalui keputusan yang telah diperoleh, penyamaan memaksa sifar berjaya direka bentuk untuk jalur mikro berkepanjangan 1 inci dan 20 inci menggunakan perancangan yang dicadangkan.
ZERO FORCING EQUALIZER FOR SIGNAL INTEGRITY APPLICATION

ABSTRACT

In today’s world, communication system with high data rate usually suffers from signal degradation such as distortion and reflection. Intersymbol interference is a signal distortion that causes heavy data loss in a communication system. The presence of intersymbol interference will result in wrongly decoded data at the receiver as the receiver cannot predict the correct level of the square waveform, leading to the loss of information. Therefore, the equalizer will be used to recover the transmitted data at the receiver. A study has been conducted in removing the intersymbol interference by applying a precursor equalizer by a time reversal and use practical minimum phase filter [1]. However, the limitation is it can only combat precursor intersymbol interference. If a signal is suffering from post-cursor intersymbol interference, this method cannot be used. Therefore, the main objective of this project is to design a zero forcing equalizer for signal integrity application that mitigates the post-cursor intersymbol interference. This project analyzes the performance of zero-forcing technique to achieve a data rate of 10.0 Giga-bit per second for single-ended signal like double data rate (DDR). The simulation will be obtained using Advanced Design System (ADS) and Matlab. For the calculation to cancel the post-cursor inter symbol interference, it will be carried out using Matlab. The quality of the signal of the equalizer in this project will be analyzed using an eye diagram. In this project, two lengths of microstrip will be used which are 1 inch and 20 inches. For each of the microstrip length, one pulse response and PRBS pattern will be used as a reference to cancel the ISI. One pulse response is used because it is the only way to find out the post-cursor ISI and to carry out the zero forcing calculation before implementing it in PRBS pattern. PRBS pattern shows the level of accuracy for zero forcing calculation whether it succeeds or not. With these results, it is concluded that zero forcing equalizer is successfully designed for microstrip length of 1 inch and 20 inches using the proposed methodology.
CHAPTER 1

INTRODUCTION

1.1 Research Background

Signal integrity carries the meaning of a digital signal that has a clean, unimpaired and fast transition; stable and have an accurate placement in time and it would be free of any transient [2]. Digital signal is basically analog in nature, and it also subjected to suffer from noise, distortion and loss. Over short conductor with low bit rates, signals usually able to be transmitted without having to suffer from effects such as distortion. However, as technology evolves, the need for high-speed signal becomes more significant. The conductor becomes longer, and the bit rates become higher. These can cause degradation to the signal to the point where some receivers fail to receive the signal transmitted or worse, a device fails to operate.

High-speed signal has become a key factor of the evolving technology. Each year, improvement is made to each high-speed signal application such as SATA I to SATA III, Thunderbolt, PCI Express and USB 3.1 SuperSpeed. All these applications can run up to 20.0 Giga-bit per second. A lot of works have to be done in order to achieve the desired specifications for these applications. Figure 1.1 on the left shows a combination of SATA III and USB 3.0 while Figure 1 on the right is Thunderbolt 3. SATA III and USB 3.0 have a data rate of 5.0 Giga-bit per second up to 6.0 Giga-bit per second while Thunderbolt 3 has data rate of 20.0 Giga-bit per second. Other high-speed application that exists is digital oscilloscopes, digital spectrum analyzer, broadband receivers and many more [3].

Figure 1.1: (a) USB 3.0 to SATA III [4] (b) Thunderbolt 3 [5]
Even though it seems like the evolving high-speed signal application is smooth sailing, there are still problems associated with high-speed signal such as reflections and distortions, crosstalk between multiple nets, rail collapse in the power and ground distribution network and electromagnetic interference (EMI) from component or system that needs to be resolved [6]. High-speed circuit designers need to consider a lot of things such as termination design and layout design when encounter with signal integrity application [7]. For this project, the transmission line is used as the conductor of the digital signal. The transmission line is defined as a “conductive connection between a transmitter and a receiver capable of carrying a signal” [8].

There are different types of transmission line such as balanced two-wire transmission line, coaxial cables and planar transmission line such as stripline and microstrip [9]. The transmission line can suffer from losses as a result of the high speed data rate that being implemented. Four types of losses that are associated with the transmission line is radiative losses, resistive and dielectric losses, cross-talk and reflection [10]. One of the many ways to recover the received signal into its original signal is by using an equalizer. An equalizer is a device that seeks to reverse the distortion caused by the signal transmitted through a channel. In digital communication, the purpose of an equalizer is to reduce the intersymbol interference (ISI) to allow the transmit symbols to be recovered.

Equalizers are divided into two types which are a linear equalizer and non-linear equalizer. It is called linear equalizer because it has no feedback path to adapt the equalizer while non-linear equalizer is fed back to change the subsequent output of the equalizer. Linear equalizer consists of zero forcing equalizer (ZFE) and minimum mean square error (MMSE) while non-linear equalizer consists of decision feedback equalizer (DFE) and maximum likelihood sequence estimator (MLSE). The advantage of the linear equalizer is its simplicity in implementing it but the drawback is linear equalizer usually suffer from noise enhancement. The reason for this problem is that in linear filtering, the desired signal and noise are processed together, hence the noise enhancement problem [11]. For non-linear equalizer, its advantages are it works well with severe ISI and it can boost high-frequency content without noise. This is because once the
information symbol that has been decided upon is detected, the ISI that induces on the future symbol can be estimated and subtracted out before detection of subsequent symbols [12]. The downside of using non-linear equalizer is there is a higher chance of error propagation because an incorrect decision may add ISI instead of removing it.

For this project, zero-forcing technique will be used to mitigate the ISI. Zero forcing equalizer refers to a form of linear equalization algorithm used in communication system which applies the inverse of the frequency response of the channel. The name zero forcing corresponds to bringing down the ISI to zero in a noise-free case [13]. The ability of the equalizer to remove ISI will be tested using the pseudo-random bit sequence (PRBS) pattern. PRBS pattern will show whether the equalizer succeeds to combat the ISI or not.

The signal quality of the zero forcing equalizer will be evaluated using an eye diagram. Eye diagram works as an indicator of the quality signal in high-speed digital transmission. The equalizer that will be designed from this project can later be used as a future reference to improve its performance in achieving higher data rates. There are many advantages of digital equalization over analog equalization. Digital equalization has better simplification of design and verification as it is less susceptible to noise and easier to lay out. It also has better flexibility and reliability because digital filters performance is relatively independent of actual component values [14].
1.2 Problem Statement

High-speed signal application has been part of the evolving technology. As years passed, higher and bigger data rate is required to operate the high-speed signal application. Even though most of the applications run smoothly, it is undeniable that some of it still suffers from signal degradation such as distortion and reflection. Reflection occurs due to the impedance mismatching of characteristic impedance and load impedance. The transmitted signal will be reflected back to its origin due to the differences in impedance along the transmission line. This will cause the receiver not able to receive the transmitted signal completely. Intersymbol interference or known as ISI is a form of distortion of a signal. One or more symbols can trespass each other that will result in noise or a less reliable signal. The main reason for the occurrence of ISI is multipath propagation or non-linear frequency in channels. This will cause a blur or a mixture of symbols, which can reduce signal clarity. This can be avoided by leaving enough space in between the transmitted symbol but the drawback is the throughput will decrease. A smarter method to overcome signal degradation is to use an equalizer which can help limit the ISI. Equalizer also found to be the best fit as it can alter signal easier to be recognized at the receiver. Zero forcing technique has been chosen because of its simplicity in implementing it and its capability of removing the intersymbol interference. Other than that, most of the references or thesis papers that can be found mostly use zero forcing in wireless applications such as Orthogonal Frequency Division Multiplexing (OFDM) and Multiple Input Multiple Output (MIMO). As the references for zero forcing equalizer for signal integrity application is limited, it appears that using this technique is appropriate and suitable as it can be used as a future reference to other people.
1.3  Research Objectives

The objectives of this project are:

- To design an equalizer with a data rate of 10 Giga-bit per second using zero-forcing technique.
- To recommend the best equalizer setting for different configurations.

1.4  Scope of Research

In this project, one pulse response is used as a reference to design an equalizer. For the channel, the characteristic impedance was set to 50 ohms. The simulation is carried out using the Advanced Design System (ADS) and Matlab. The length of the microstrip is varied to 1 inch, 5 inches, 10 inches, 15 inches and 20 inches. After the channel analysis has been completed, the presence of intersymbol interference (ISI) will be analyzed from the result of the one pulse response by setting the load impedance to 120 ohms. This was chosen based on the worst case termination. For equalizer design, only two lengths that will be used which are 1 inch and 20 inches. The calculations for zero forcing will be carried out in the Matlab in order to cancel out the post-cursor ISI. After that, the equalizer will be tested on pseudo-random bit sequence (PRBS) pattern to see whether it succeeds or not. This project will only cover the signal integrity of the transmission line and whether the designed zero forcing equalizer can cater to different configurations.
1.5 Thesis Outline

This thesis is divided into five main chapters. Research background, problem statement, research objectives, research scopes and thesis outline are described in Chapter 1. Chapter 2 consists of a literature review which described the related work that relevant to background studies. It provides the summary, description, analysis and critical evaluation of the past works. Then, the methodology of research which included project overall flow and experimental procedure will be explored in Chapter 3. The presence of intersymbol interference (ISI) is explained and the calculations to remove ISI are presented. After that, Chapter 4 is the results and discussions that provide the analysis and discussions of the result and findings. The design of the equalizer is carried out. Limitation of the designed equalizer is also discussed in this chapter. The performance of the equalizer for different configuration is also reviewed. Finally, Chapter 5 contains a conclusion that summarizes the overall of the project and provides some recommendations for future improvements.
CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In digital communication, the purpose of an equalizer is to reduce the inter symbol interference (ISI) to allow the transmit symbols to be recovered. There are plenty of equalizers such as minimum mean square error (MMSE) equalizer, decision feedback equalizer (DFE), continuous time linear equalizer (CTLE) and many more. There are many advantages of digital equalization over analog equalization. Digital equalization has better simplification of design and verification as it is less susceptible to noise and easier to lay out. In this project, zero-forcing technique will be used as it is the simplest to implement and to understand conceptually.

2.2 Transmission Line Theory

The main difference between circuit theory and transmission line theory is the electrical size. The transmission line may be a considerable fraction of a wavelength or many wavelengths in size thus it is a distributed-parameter network, where currents and voltages can vary in phase and magnitude over its length [15]. Transmission line for transverse electromagnetic (TEM) wave propagation always has at least two conductors. One of the example of TEM wave propagation is coaxial cable where the magnetic field and electrical field is perpendicular to each other and it perpendicular to the direction of propagation. The transmission line is often schematically represents by two wire-line as depicted in Figure 2.1.

![Figure 2.1: Two wire-line [15]](image)
The piece of line of infinitesimal length $\Delta z$ can be modelled as a lumped-element circuit as depicted in Figure 2.2.

![Figure 2.2: Lumped-element circuit [15]](image)

The shunt capacitance $C$ is due to the close proximity of the two conductors and the series inductance $L$ represents the total self-inductance of the two conductors. The series resistance $R$ represents the resistance due to the finite conductivity of the conductors, and the shunt conductance $G$, is due to dielectric loss in the material between conductors. $R$ and $G$ therefore represents loss. But in this project, microstrip is used as the channel. In microstrip, it has Quasi TEM where the term quasi means the wave resembles the TEM wave. Since microstrip consists of dielectric part in the middle and conductor part at the top and bottom, wave propagates through the conductor part at the top and through the dielectric substrate. Hence the term Quasi TEM since the wave propagates with different speeds through two different mediums having different resistivity.

2.3 Signal Integrity

Greater design complexity, accelerating data rates, standards requirements and shorter cycle put a greater demand on design engineers to debug complex signal integrity issues as early as possible. Plenty of variables can affect the signal integrity including transmission line effects, signal routing, impedance mismatches, termination schemes and grounding schemes since serial data links operate at gigahertz transmission frequencies. A serial digital signal that travels from the transmitter to receiver can suffer from impairments. The transmitter, connectors, PCB traces and cables will introduce interference that will degrade a signal both in its amplitude and timing.
There are many signal integrity issues that printed circuit board (PCB) design engineers need to consider when designing a high speed channel. Band-limited wire line interconnects can be found in various high-performance digital systems—from backplanes of high-speed internet routers, to server/rack backplanes in data centers, to processor-memory interfaces in modern portable and desktop computers [16]. All these devices are limited by the same channel issues such as dielectric and skin loss, connector cross-talk and impedance discontinuities as they try to reach high data rates. Various equalization techniques can be utilized to overcome these issues.

2.4 Fringing Field Microstrip

The fringing electric field is the field that exists at the edges of parallel plate capacitor where the electric field between the parallel plates of the capacitor will be perpendicular to the plates and originating from the positive one and ending at the negative one. Microstrip antenna’s radiation arises from the fringing fields, which is due to the advantageous voltage distribution [17]. Microstrip patch antenna radiates fringing field between the peripheries patch and ground plane. The fringing fields are enhanced by decreasing the εr or increasing the substrate thickness, H [18]. However, for the microstrip transmission line where there is no power is to be radiated, a high value of εr is desired. This is because the fields are more tightly contained hence less fringing and resulting in less radiation.

2.5 Transmission Channel

A representative depiction of a communication link between two chips is shown in Figure 2.3. Dedicated circuits designed for high-speed operation are used as transmitter and receiver, to transmit and receive the data, respectively. The medium of transmission is called the channel which in the ideal case is a wire representing a short circuit. However, as the data rates increase, these wires behave as lossy transmission lines severely degrading the transmitted data symbols. Equalization is a well-known technique used to overcome non-idealities introduced by the channel. Several equalization techniques that are amenable for high-speed operation is presented.
Based on the target application, there are few types of channels used in high-speed interconnects. These channels are classified into three categories. Firstly, for chip-to-chip communication on a printed circuit board (PCB), short well-controlled copper traces are used. Then, for systems such as local area network (LAN) which require a high-speed connection between two computers, coaxial cable is used as the transmission medium. Finally, for high-speed board-to-board communication systems such as routers, copper traces along with backplane connectors are used. The copper traces commonly used on PCBs behave as a lossy transmission lines at multi-gigahertz frequency range.

The geometry of the traces has been one of the reasons for frequency dependent loss mechanism, making the development of a generic channel model impractical. Due to this issue, channel models are usually developed by fitting measured data of each of the components. For example, the s-parameters of the PCB trace with a given geometry are determined by using field solvers such as Advanced Design System and combined with connector models supplied by the vendor to obtain the s-parameters for the complete channel [19].
2.6 S-Parameter

Scattering parameter or know as S-parameter is a mathematical construct that quantifies how radio frequency (RF) energy propagates through a multi-port network. It is a useful method for representing a circuit as ‘black box’.

![Figure 2.4: Representation of a black box (redraw from [20])](image)

S-parameter is measured by sending a single frequency signal into the ‘black box’ and detecting what waves exit from each port. Some waves reflect back out of the port and some portion of the signal exits through other port as depicted in Figure 2.5.

![Figure 2.5: Reflection and transmission of wave (redraw from [20])](image)

S-parameters are dependent upon the source and load impedances. In this project, two parameters that will be analyzed is $S_1$ and $S_2$. $S_1$ refers to the signal reflected at Port 1 for the signal incident at Port 1 or known as reflection coefficient. $S_2$ refers to a signal exiting at Port 2 for signal incident at Port 1 or knows as transmission coefficient.
Two port parameters are defined for a general 2-port network as shown in Equation 2.1 below [22]:

\[
\begin{bmatrix}
 b_1 \\
 b_2
\end{bmatrix} =
\begin{bmatrix}
 S_{11} & S_{12} \\
 S_{21} & S_{22}
\end{bmatrix}
\begin{bmatrix}
 a_1 \\
 a_2
\end{bmatrix}
\]

\[b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2 = S_1 \cdot a_1 \quad \Rightarrow \quad S_1 = \left. \frac{b_1}{a_1} \right|_{z_1 = z_0}
\]

\[b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2 = S_2 \cdot a_1 \quad \Rightarrow \quad S_2 = \left. \frac{b_2}{a_1} \right|_{z_1 = z_0}
\]

Equation 2.1: General two-port network

2.7 Impedance Mismatching

It is vital to have zero or minimum power loss when transferring radio frequency (RF) energy to load through transmission lines. In order to achieve this, it is important for the source and load impedances to be matched. The transmission line between the source and load should also have equal characteristics impedances. However, impedance mismatch in the transmission line will cause some of the signal power reaching to the load to be reflected back and produce a standing wave. For a power amplifier of a transmitter, impedance mismatch can cause a huge impact on the power loss, maximum reachable output power and linearity [23].
2.8 Intersymbol Interference (ISI)

Intersymbol interference (ISI) is a signal distortion in telecommunication. Noise or less reliable signal can be caused when one symbol or more interfere with each other. Multipath propagation or non-linear frequency in the channel is the main reason for the presence of ISI. With the use of adaptive equalization method and error correcting codes, error rates from the ISI can be minimized. Post-cursor ISI is caused by the past bits whereas precursor ISI is caused by the future bits on the present bits.

![Figure 2.7: Precursor and post-cursor ISI](image)

According to [25], two approaches are implemented in order to mitigate the known interference. One is using linear methods such as tapped delay lines and the other is to minimize error without linearity constraint. Out of these two approaches, the non-linear detector seems to be the best fit as it minimizes the expected number of errors by detecting a single sequence of \( n \) transmitted symbol. The detector made decisions based on the received symbol.

2.9 Pseudo Random Bit Sequence

Pseudo Random Bit Sequence (PRBS) is a pattern test that seems to be random but actually a repeatable and predictable bits. It consists of only two bits of 0 and 1. Generally, the common PRBS pattern that represents polynomials are PRBS7, PRBS9, PRBS11 and so on [26]. The PRBS has the maximum length of \( 2^k - 1 \) sequences and \( k \) means the size of unique data in the sequence. As an example for PRBS7, it has 127 bits while for PRBS9, it has 511 bits. PRBS
is widely used for testing the correct functionality of high-speed digital circuits [27]. It is also used to generate an eye diagram.

2.10 Eye Diagram

By using eye diagram, the system performance can be quickly evaluated. The eye diagram is a common indicator of the signal quality in high-speed digital transmissions. The eye diagram is generated by overlaying sweeps of different segments of a long data stream driven by a master clock. The triggering edge can be positive or negative, but the displayed pulse that appears after a delay period may go either way; there is no way of knowing beforehand the value of an arbitrary bit [28]. Therefore, when many such transitions have been overlaid, positive and negative pulses are superimposed on each other. Overlaying many bits produces an eye diagram, so called because the resulting image looks like the opening of an eye.

A properly constructed eye should contain every possible bit sequence from simple alternate 1’s and 0’s to isolated 1’s after long runs of 0’s, and all other patterns that may show up weaknesses in the design. Eye diagrams usually include voltage and time samples of the data acquired at some sample rate below the data rate. In Figure 2.8, the bit sequences 011, 001, 100, and 110 are superimposed over one another to obtain the final eye diagram.

![Figure 2.8: Formation of eye diagram](image-url)
As can be seen in Figure 2.9, an eye diagram can reveal important information. It can indicate the best point for sampling, divulge the SNR (signal-to-noise ratio) at the sampling point, and indicate the amount of jitter and distortion. Additionally, it can show the time variation at zero crossings, which is a measure of jitter.

Figure 2.9: Information on eye diagram [28]

Eye diagrams provide instant visual data that engineers can use to check the signal integrity of a design and uncover problems early in the design process. Used in conjunction with other measurements such as bit-error rate, an eye diagram can help a designer predict performance and identify possible sources of problems.

2.11 Equalizer

In digital communication, the idea goal is the reliable transmission of the information at the highest possible data rates. However, when the high-speed data is transmitted over the communication channel, intersymbol interference (ISI) will occur. In order to mitigate the effect of ISI, equalization technique is used at the receiver. The purpose of the equalizer is to reverse the effect that the channel has on the transmitted signal in order to reproduce the original signal at the receiver end. An equalizer is divided into two techniques which are linear equalizer and non-linear equalizer [12]. A linear equalizer is suboptimal but simple to implement. A non-linear equalizer is for severe and noisy channels.

For this project, zero forcing equalizer is used to combat the ISI on the transmitted signal. Zero forcing equalizer refers to a form of linear equalization algorithm which
applies the inverse of the frequency response of the channel used in communication systems [30].

Zero forcing aims to bring down the ISI to zero, only if the ISI is significant compared to noise. The zero forcing equalizer $C(f)$ is constructed as shown in Equation 2.2:

$$C(f) = \frac{1}{F(f)}$$

Equation 2.2: Zero forcing equalizer

Where $F(f)$ is for the channel with frequency response. Hence the combination of zero forcing equalizer and channel response will produce flat frequency response and linear phase $C(f)F(f) = 1$.

2.12 Previous Work

According to a journal titled Precursor Inter-Symbol Interference Removal by Block Transmission-Based Time-Reversed Equalization [31], zero forcing equalizer is implemented to cancel the precursor intersymbol interference (ISI) using matched filtering and simple linear equalizer. A scheme called block transmission-based time-reversed equalization (BT-RTE). The primary idea is to adopt block transmission and apply precursor equalizer by a time reversal and use practical minimum phase filter. Using this scheme, the precursor ISI can be removed completely.

![Proposed equalization scheme](redraw from [31])

Based on Figure 2.10, on the transmitter side, the transmitted data symbol is sent in block. While at the receiver side, each block is reversed in time, fed through a filter with the transfer function of $\left(M'(z^*)\right)^{-1}$ and it is reversed back in time. Note that $M(z)$ is a minimum phase, $M'(z^*)$ is also minimum phase, hence $\left(M'(z^*)\right)^{-1}$ is practical. This three step procedure is a
realization of the precursor equalizer \( \left( M'(z^*) \right)^{-1} \). In this project, zero forcing equalizer is proposed to be applied at the transmitter side to mitigate the postcursor ISI. In order to cancel the postcursor ISI, a calculation is carried out using the equation:

\[
X = q
\]

Equation 2.3: Zero forcing equalizer

Where \( X \) is in matrix form and represents the values for postcursor ISI, \( \mathcal{L} \) is the coefficients that will be used to cancel the postcursor ISI and \( q \) is the desired pulse output. This equation is used to achieve an ISI-free transmitted signal.

2.13 Summary

In this chapter, the background of transmission line theory, transmission channel and s-parameter had been reviewed. Impedance mismatching can cause reflection on the signal. PRBS pattern is used to generate the eye diagram to measure the quality of the signal. The previous works focused on removing the precursor ISI and suggested of using matched filtering and simple linear equalizer.
CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter reviews the methodology to design a zero forcing equalizer. For this part, all the simulations were done in Advanced Design System or known as ADS. Simulations on frequency domain, time domain, termination, pseudo-random bit sequence (PRBS) pattern and eye diagram were included. The calculation on zero forcing was carried out in Matlab. This chapter reviewed all the important parameters done to design an equalizer.

3.2 Project Flow

Before starting with this project, all the types and techniques of equalizers are being studied first. After the technique to be used in designing the equalizer has been decided to, the next step is to design the channel and microstrip is used for the transmission line. Frequency domain and time domain will be used to analyze the result of the channel. The value for characteristic impedance has been set to 50 ohms and microstrip length was adjusted from 1 inch to 20 inches. The initial length for the microstrip is set to be 1 inch but will increase gradually. After that, ADS will be used to run the simulation and to see whether inter symbol interference or other issues occur. If any issues occur, the coefficients will be calculated in order to remove the inter symbol interference. Equalizer will be designed using Matlab. The equalizer will be analyzed whether it can be used for a different configuration. It is also possible that there would be limitations regarding the equalizer. Figure 3.1 shows the flowchart of this project.
Figure 3.1: Flowchart of the methodology
3.3 Channel Design

Channel design gave a visualization on how the signal is transmitted from the transmitter to the receiver through the channel. Most of the signal usually suffered from signal degradation that caused the received signal to be different compared to the transmitted signal.

![Channel design](image)

Figure 3.2: Channel design

In this project, point-to-point topology is used as in Figure 3.2. For the transmission channel, microstrip with FR4 substrate is used since it has excellent mechanical properties [32]. For a FR4 substrate, its dielectric constant used is 4.4.

![Microstrip structure](image)

Figure 3.3: Structure of microstrip (redraw from [33])

Figure 3.3 shows the structure of a microstrip. All the parameters are filled in order to achieve the desired value of the characteristic impedance.
Simulation in ADS

3.4.1 Characteristic Impedance

The most important setting for microstrip is to set its characteristic impedance to a value that will suit the transmission channel. For this transmission channel, 50 ohms has been chosen as the ideal value. In order to achieve the value for the characteristic impedance, certain parameters are filled in accordingly. In this simulation, the value for each parameter is set as in Table 3.1:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>H, the thickness of the substrate</td>
<td>6 mil</td>
</tr>
<tr>
<td>( \varepsilon_r ), dielectric constant</td>
<td>4.4</td>
</tr>
<tr>
<td>T, the thickness of strip metallization</td>
<td>1.7 mil</td>
</tr>
<tr>
<td>TanD, dielectric loss tangent</td>
<td>0.02</td>
</tr>
<tr>
<td>W, the width of the strip</td>
<td>10 mil</td>
</tr>
</tbody>
</table>

Table 3.1: Parameters for characteristic impedance
Figure 3.4 shows the LineCalc section in ADS. Through this tool, the characteristic impedance is set to 50 ohms. Equation 3.1 and Equation 3.2 are used to calculate the characteristic impedance, $Z_0$ manually. From this equation, the value for characteristic impedance is 54.4 ohm.

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + \frac{12d}{W}}}$$

Equation 3.1: Effective dielectric constant

$$Z_c = \frac{120\pi}{\sqrt{\varepsilon_e \cdot \varepsilon_r} \left[ \frac{W}{d} + 1.393 + 0.667 li \left( \frac{W}{d} + 1.444 \right) \right]}$$

Equation 3.2: Characteristic Impedance

3.4.2 Length of Microstrip

As for the L, length of the microstrip, it will vary from 1 inch, 5 inches, 10 inches, 15 inches and 20 inches. For the transmission line, the length of the microstrip cannot be too short as the signal might not be sensitive enough with some of the important properties that are related to it [34]. Figure 3.5 shows the schematic diagram of the transmission line channel in ADS.

Figure 3.5: Schematic diagram in ADS
3.5 Frequency Domain

The frequency domain is used to analyze the return loss and insertion loss of a signal.

3.5.1 S-Parameter

Figures below show the result of S-Parameter for different lengths. In this section, the load impedance and characteristic impedance have the same value of 50 ohms.

![Figure 3.6: $S_1$ and $S_2$ for L=1 inch](image)

![Figure 3.7: $S_1$ and $S_2$ for L=5 inches](image)

![Figure 3.8: $S_1$ and $S_2$ for L=10 inches](image)
Figure 3.9: $S_1$ and $S_2$ for L=15 inches

Figure 3.10: $S_1$ and $S_2$ for L=20 inches

$S_1$ represents how much power is reflected, hence known as the reflection coefficient or return loss. Return loss is a measure of how well devices or lines are matched. The match is considered good if the value for return loss is high since high return loss is desirable, resulting in lower insertion loss. $S_2$ usually associated with insertion loss. It is also referred to as transmission coefficient because they refer to what happen from one port to another. Insertion loss is the loss of signal power resulting from the insertion of a device in a transmission line.
<table>
<thead>
<tr>
<th>Length (inch)</th>
<th>$S_1$ (dB)</th>
<th>$S_2$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-41.474</td>
<td>-0.354</td>
</tr>
<tr>
<td>5</td>
<td>-43.120</td>
<td>-1.770</td>
</tr>
<tr>
<td>10</td>
<td>-47.474</td>
<td>-3.540</td>
</tr>
<tr>
<td>15</td>
<td>-47.574</td>
<td>-5.310</td>
</tr>
<tr>
<td>20</td>
<td>-45.808</td>
<td>-7.080</td>
</tr>
</tbody>
</table>

Table 3.2: Values for $S_1$ and $S_2$ for different lengths

Based on Table 3.2, all the values are taken at 5 GHz. For $S_1$, the value decreases when the length increases. The desirable value for return loss is supposedly high. Therefore, for all the lengths listed above, all the lengths are considered as desirable. This is because, any value that is below than -40 dB is considered as good as there is almost no loss occur. This is also as a result from a matching value between characteristic impedance and load impedance. As for $S_2$, the desirable value for insertion loss is low for better performance [35]. From the table above, the value decreases when the length increases. The desirable value for $S_2$ is -0.354 dB with the length of microstrip of 1 inch as it is closer to 0 dB.

For this section, the value for characteristic impedance and load impedance did not match. The value for characteristic impedance is still fixed to 50 ohms but the value for load impedance has been changed 30 ohms, 70 ohms and 120 ohms.
<table>
<thead>
<tr>
<th>Length (inch)</th>
<th>$S_1$ (dB)</th>
<th>$S_2$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-6.853</td>
<td>-1.398</td>
</tr>
<tr>
<td>5</td>
<td>-8.300</td>
<td>-2.616</td>
</tr>
<tr>
<td>10</td>
<td>-12.306</td>
<td>-4.039</td>
</tr>
<tr>
<td>15</td>
<td>-12.417</td>
<td>-5.819</td>
</tr>
<tr>
<td>20</td>
<td>-10.792</td>
<td>-7.731</td>
</tr>
</tbody>
</table>

Table 3.3: Values for $S_1$ and $S_2$ for load impedance of 30 ohms

<table>
<thead>
<tr>
<th>Length (inch)</th>
<th>$S_1$ (dB)</th>
<th>$S_2$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-10.141</td>
<td>-0.816</td>
</tr>
<tr>
<td>5</td>
<td>-11.702</td>
<td>-2.147</td>
</tr>
<tr>
<td>10</td>
<td>-15.885</td>
<td>-3.746</td>
</tr>
<tr>
<td>15</td>
<td>-16.005</td>
<td>-5.536</td>
</tr>
<tr>
<td>20</td>
<td>-14.293</td>
<td>-7.361</td>
</tr>
</tbody>
</table>

Table 3.4: Values for $S_1$ and $S_2$ for load impedance of 70 ohms
Table 3.5: Values for $S_1$ and $S_2$ for load impedance of 120 ohms

<table>
<thead>
<tr>
<th>Length (inch)</th>
<th>$S_1$ (dB)</th>
<th>$S_2$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-3.310</td>
<td>-3.218</td>
</tr>
<tr>
<td>5</td>
<td>-4.484</td>
<td>-4.162</td>
</tr>
<tr>
<td>10</td>
<td>-7.865</td>
<td>-4.961</td>
</tr>
<tr>
<td>15</td>
<td>-8.038</td>
<td>-6.803</td>
</tr>
<tr>
<td>20</td>
<td>-6.619</td>
<td>-8.921</td>
</tr>
</tbody>
</table>

Table 3.3, Table 3.4 and Table 3.5 show the values for $S_1$ and $S_2$ for different lengths with load impedance of 30 ohms, 70 ohms and 120 ohms respectively. All these values were taken at the frequency of 5 GHz. In general, for $S_1$ and $S_2$ the value decreases with higher lengths. It is also known that higher value is desirable for return loss. Therefore, for all three different terminations, the most desirable length for $S_1$ is 1 inch. For $S_2$, the desirable value for insertion loss is supposedly low. The most desirable length for $S_2$ is 1 inch since all the values for 1 inch is closest to 0.
3.6 Time Domain

The time domain is used to generate the one pulse response for different length of microstrip. Each pulse response behaved differently with different lengths.

3.6.1 One Pulse Response

Figure 3.11 shows the schematic diagram of a transmission line to get one pulse response. In this diagram, it shows that the pulse width parameters had been set to certain values in order to meet the requirements. The microstrip, MLIN had been set to impedance of 50 ohms. The load impedance also had been set to 50 ohms. This is to avoid impedance mismatch that can cause standing wave as a result of signal power reaching the load to be reflected back.

Figure 3.11: Schematic diagram for one pulse response
<table>
<thead>
<tr>
<th>Length (inch)</th>
<th>Vin</th>
<th>Vout</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><img src="image" alt="Graph" /></td>
<td><img src="image" alt="Graph" /></td>
</tr>
<tr>
<td>5</td>
<td><img src="image" alt="Graph" /></td>
<td><img src="image" alt="Graph" /></td>
</tr>
<tr>
<td>10</td>
<td><img src="image" alt="Graph" /></td>
<td><img src="image" alt="Graph" /></td>
</tr>
<tr>
<td>15</td>
<td><img src="image" alt="Graph" /></td>
<td><img src="image" alt="Graph" /></td>
</tr>
<tr>
<td>20</td>
<td><img src="image" alt="Graph" /></td>
<td><img src="image" alt="Graph" /></td>
</tr>
</tbody>
</table>

Table 3.6: Figures for one pulse response for Vin and Vout
Based on Table 3.6 for Vin column, it can be seen that all the pulses remain at the same place regarding of its length. Differ from Vout column, each pulse is getting farther away from the starting point as the length increases. This shows that the length of the transmission channel will cause delay for the output pulse. The pulse height also getting shorter when the length increases.

3.6.2 Termination

Electrical termination is a method used to end a transmission line using a device that matches the characteristics impedance of the microstrip. Termination is important in every transmission line in order to avoid reflection. Reflection can happen when the far end of the line is not properly terminated in its characteristic impedance. In this project, the characteristic impedance is 50 ohms, therefore the right termination value for the resistor at the right end is also 50 ohms for its impedance. In this section, the impedance value for the resistor at the right end is changed to 70 ohms, 120 ohms and 30 ohms to show that the signal will suffer from reflection.

Figure 3.12: Schematic diagram for a load impedance of 70 ohm
Figure 3.12 shows the value for the impedance load at the right end is changed to 70 ohms to show the changes in response when the load impedance differs from the characteristic impedance.

![Figure 3.12](image)

Figure 3.13: Pulse response for L= 1 inch

Figure 3.13 shows the one pulse response of the signal when the load impedance is changed to 70 ohms. In this simulation, the microstrip length was set to 1 inch. From the graph, it can be seen that the signal suffered from distortion. The distortion is part of precursor and post-cursor ISI. But from the figure above, it can be seen that the purple graph suffered more on the post-cursor ISI. When the termination is carried out, the load impedance has to match the characteristic impedance. When these two does not match, it is not possible for all the power to be transmitted. As the power cannot disappear, it will travel back along the transmission line and back towards the source. When this happens, the voltages and currents add or subtract at different points according to the phases. The standing waves are set up in this way.

![Equation 3.3](image)

\[ V_{swr}^i = \frac{1 + |\Gamma|}{1 - |\Gamma|} \]

Equation 3.3: Equation of voltage standing wave ratio (VSWR)

Equation 3.3 is used to calculate the voltage of the standing wave ratio. This explains what happen to the Vout when the load impedance does not match with the
characteristic impedance. This also applies to the signal response of 120 ohms termination and 30 ohms termination that will be discussed after this.

Table 3.7: Pulse response for different lengths of microstrip with the termination of 70 ohms

Table 3.7 shows the pulse response for 70 ohms load impedance with different lengths. Based on the graph, it can be seen that the output pulse is getting further away as length increases. Each of post-cursor ISI also has more distance between each other.
Figure 3.14 shows the schematic diagram for a load impedance of 120 ohms. Other parameters are still the same as the previous schematic diagram; Figure 22.

Figure 3.14: Schematic diagram for a load impedance of 120 ohm

Figure 3.15 shows the signal response for load impedance of 120 ohm with microstrip length of 1 inch. From the graph, the post-cursor ISI can be clearly seen and it is more distorted than the previous signal with the same length of the transmission line;

Figure 3.15: Pulse response for L= 1 inch
Figure 3.13. The post-cursor also occurs more as the load impedance is higher. This shows that reflection is also higher for this simulation.

Table 3.8: Pulse response for different lengths of microstrip with the termination of 120 ohm

Table 3.8 shows the pulse response for 120 ohms load impedance with different lengths. Based on the graph, it can be seen that the output pulse is more distorted and further away from the input pulse. The distortion can be clearly seen and the cursor also getting narrower with increasing length.

Figure 3.16 shows the schematic diagram for load impedance of 30 ohms. Since the value of load impedance is still different from the value of characteristic impedance, signal distortion still occurred.
Figure 3.16: Schematic diagram for load impedance of 30 ohm

Figure 3.17: Pulse response for $L=1$ inch

Figure 3.17 shows the signal response for load impedance of 30 ohms with microstrip length of 1 inch. As the value for load impedance is smaller than the value of characteristic impedance, the output pulse’s height also shorter compared to the input pulse. Also, all the post-cursor reflected to the positive value, differ from two previous graphs for 70 ohms and 120 ohms.
Table 3.9: Pulse response for different lengths of microstrip with the termination of 30 ohms

Table 3.9 shows the pulse response for 30 ohms load impedance with different lengths. Based on the graph, it can be seen that as the length increases, delay between output pulses to input pulse also increases. The gap between each postcursor ISI in all the figures also getting wider and the height of each cursor is slightly decreasing when the microstrip length is increasing.

3.6.3 PRBS Pattern

PRBS stands for pseudo-random bit sequence. PRBS pattern is a sequence of random bits of 1 and 0. It is used as a test pattern and also to generate eye diagram.

3.6.3.1 Impedance Matching

Impedance matching is when the characteristic impedance had the same value with the load impedance. For this part, both impedances were 50 ohms. Figure
3.18 shows that schematic diagram for PRBS pattern. The bit sequence is set to a random bit between 1 and 0.

**Figure 3.18: Schematic diagram for PRBS pattern**

![Schematic diagram for PRBS pattern](image)

**Figure 3.19: Generated pulses of PRBS pattern**

![Generated pulses of PRBS pattern](image)

Based on Figure 3.19, the pulse is generated between 0V to 1V, according to bit sequence that has been set earlier; Figure 3.18. This generated pulse produced eye diagram as in Figure 3.20.
The eye diagram looked like the opening of an eye; hence the name. The eye diagram pattern looked neat because the termination is being done the right way. In order to get a proper eye diagram, the value for load impedance must match with characteristic impedance. Table 3.10 shows the values for eye height and eye width of the above eye diagram.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>0.973</td>
</tr>
<tr>
<td>Eye Width</td>
<td>9.977e-011</td>
</tr>
</tbody>
</table>

Table 3.10: Values for eye height and eye width

3.6.3.2 Impedance Mismatching

Impedance mismatching is when the load impedance did not match with the characteristic impedance. For this part, 120 ohms had been chosen as the worst case termination to see how the PRBS pattern and the eye diagram would look like.
Based on Figure 3.22, the pulse is generated between 0V to 1V, according to bit sequence that has been set earlier; Figure 3.21. In this schematic, the load impedance is changed to 120 ohms. This is to show what will happen to the eye diagram when impedance mismatch happened as in Figure 3.23.
Figure 3.23: Eye diagram

The eye diagram does not look like the one in Figure 3.20. The eye diagram pattern looks scattered and messy because the termination is being done the wrong way. In order to get a proper eye diagram, the value for load impedance must match with characteristic impedance. Table 3.11 shows the values for eye height and eye width of the above eye diagram.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>0.546</td>
</tr>
<tr>
<td>Eye Width</td>
<td>7.716e-011</td>
</tr>
</tbody>
</table>

Table 3.11: Values for eye height and eye width
3.7  Worst Case Termination

Figure 3.24 shows the pulse signal for worse case termination with a load impedance of 120 ohms. As can be seen from the graph, there are post-cursor ISI. These post-cursor values will be used in the calculation to cancel the ISI.

Figure 3.24: Impedance mismatch with load impedance of 120 ohms

Figure 3.25: Values for post-cursor ISI
Figure 3.25 shows the values for each post-cursor ISI. The main objective of this calculation is to achieve an ISI-free pulse signal. The calculation will be done using Matlab. Equation 3.4 is used to determine the coefficient.

\[ X = q \]

Equation 3.4: Zero Forcing Equalizer [36]

Where \( X \) ws the values of postcursor ISI, \( C \) is the coefficient that will be determined later and \( q \) is the desired pulse output.

<table>
<thead>
<tr>
<th>Coefficients</th>
<th>Value of postcursor ISI</th>
<th>Pulse Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>1.4</td>
<td>1</td>
</tr>
<tr>
<td>M2</td>
<td>-0.57</td>
<td>0</td>
</tr>
<tr>
<td>M3</td>
<td>0.23</td>
<td>0</td>
</tr>
<tr>
<td>M4</td>
<td>-0.09</td>
<td>0</td>
</tr>
<tr>
<td>M5</td>
<td>0.03</td>
<td>0</td>
</tr>
<tr>
<td>M6</td>
<td>-0.01</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3.12: Values from the graph
Based on the calculations done, Table 3.13 shows the values for each coefficients. These values will be used to cancel the postcursor ISI.

Table 3.13: Values for each coefficients

<table>
<thead>
<tr>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7143</td>
<td>0.2908</td>
<td>0.0011</td>
<td>-0.0014</td>
<td>0.0026</td>
<td>0.0002</td>
</tr>
</tbody>
</table>

3.8 Summary

In this chapter, the overall methodology is reviewed and analyzed. The main focus of chapter three is to prove the calculation for zero forcing can be carried out in order to cancel the post-cursor ISI and to design the equalizer. In this chapter, all the data and graphs are analyzed to show that the distortion or post-cursor ISI can be mitigated. Then, from all these graphs, it can be concluded that the termination played an important role in the appearance of post-cursor ISI. This chapter also reviewed the eye diagram to show the importance of impedance matching to get a good signal quality.
CHAPTER 4
RESULTS AND DISCUSSION

4.1 Introduction

This chapter discussed on simulations obtained through Matlab. In the previous chapter, all the simulations were done in ADS except for the zero forcing calculation. All the simulations in ADS were converted into ASCII and CSV file format in order to obtain the exact same simulation when plotted in Matlab. For this part, two lengths of microstrip have been chosen to be analyzed in order to design a zero forcing equalizer. The first length would be 1 inch and the second one is 20 inches with 120 ohms termination for both lengths. This is based on the worst case termination as 120 ohms suffers more of post-cursor ISI compared to 30 ohms and 70 ohms.

4.2 One Pulse Response

The main reason for plotting a one pulse response is to be able to analyze the post-cursor ISI as this is the only way of obtaining the accurate value of the postcursor. This simulation was first obtained in ADS before converted it into ASCII and CSV file format in order to plot it in Matlab.

![Figure 4.1: One pulse response for microstrip with a length of 1 inch](image)
Figure 4.2: One pulse response for microstrip with a length of 20 inches

Figure 4.1 and Figure 4.2 shows the one pulse response of microstrip with a length of 1 inch and 20 inches respectively. Based on the graphs above, post-cursor ISI can be clearly seen. The signal was not smooth and has distortion. These simulations will be used to implement a zero forcing equalizer in order to cancel the post-cursor ISI.

4.3 Desired One Pulse Response

Desired one pulse response was used as a reference on how the one pulse response should look like after it went through the equalization process.

Figure 4.3: Desired one pulse response for microstrip with a length of 1 inch
Figure 4.4: Desired one pulse response for microstrip with a length of 20 inches

Figure 4.3 and 4.4 show the desired one pulse response for microstrip with a length of 1 inch and 20 inches respectively. In order to obtain this desired one pulse response, sampling time was taken and at each sampling time, it will be set to either 0V or 1V. In both simulations, the sampling time taken was \(100 \times 10^{-1}\) second.

4.4 One Pulse Response with Equalizer

This part shows the final result of one pulse response after underwent a zero forcing calculation and to see whether the post-cursor ISI can be successfully mitigated or not.

Figure 4.5: One pulse response without equalizer and with equalizer for microstrip length of 1 inch
Figure 4.6: One pulse response without equalizer and with equalizer for microstrip length of 20 inches

Figure 4.5 and Figure 4.6 shows the comparison of one pulse response without equalizer and with equalizer for microstrip length of 1 inch and 20 inches respectively. For figure 4.5, the red graph represents the one pulse response before equalization while the blue graph represents the one pulse response after equalization. For Figure 4.6, the blue graph represents the one pulse response before equalization and the red graph represents the one pulse response after equalization. Based on the two figures above, the post-cursor ISI had been successfully cancelled. However, this is not the final result to design the zero forcing equalizer since it had not been tested yet using the PRBS pattern.
4.5 PRBS Pattern

PRBS pattern or known as pseudo-random bit sequence pattern is used to test the accuracy of the zero forcing equalizer. For this part, PRBS 7 is used as the bit sequence.

4.5.1 1 Inch

The figures below show the graph of PRBS pattern for microstrip with a length of 1 inch.

Figure 4.7: PRBS pattern for microstrip with a length of 1 inch

Figure 4.8: Improved PRBS pattern for microstrip with a length of 1 inch
Figure 4.7 and Figure 4.8 shows the PRBS pattern without equalizer and with equalizer respectively. In Figure 4.7, it can be seen that the graph stretched up to more than 1.5V and went to below than 0V, more than -0.5V. In Figure 4.8, the graph shows a tremendous improvement since it went only between 0V to 1V even though there was some part that went a little bit over 1V.

Figure 4.9: Comparison of PRBS pattern with equalizer, without equalizer and desired PRBS

Figure 4.9 shows the comparison between PRBS pattern without equalizer, PRBS pattern with equalizer and desired PRBS pattern. The blue graph represents the PRBS pattern without equalizer, the green graph represents the PRBS pattern with equalizer and the red graph represents the desired PRBS pattern. The desired PRBS pattern is obtained from ADS, with impedance matching meaning no ISI involved. It can be seen that the difference between the red graph and the green graph was not obvious. It had improved so much compared to the blue graph. Based on this, it can be said that the zero forcing calculation was successful for microstrip with a length of 1 inch.
4.5.2 20 Inches

The results below show the graph of PRBS pattern for microstrip with a length of 20 inches.

![Figure 4.10: PRBS pattern for microstrip with a length of 20 inches](image)

Figure 4.10: PRBS pattern for microstrip with a length of 20 inches

![Figure 4.11: Improved PRBS pattern for microstrip with a length of 20 inches](image)

Figure 4.11: Improved PRBS pattern for microstrip with a length of 20 inches

Figure 4.10 and Figure 4.11 shows the PRBS pattern without equalizer and with equalizer respectively. In Figure 4.10, it can be seen that the graph stretched up to 1.5V and down to almost -0.5. In Figure 4.11, the graph shows improvement even though there was some point that almost reached up to 1.1V and -0.3V.
Figure 4.12: Comparison of PRBS pattern with equalizer, without equalizer and desired PRBS

Figure 4.12 shows the comparison between PRBS pattern without equalizer, PRBS pattern with equalizer and desired PRBS pattern. The blue graph represents the PRBS pattern without equalizer, the green graph represents the PRBS pattern with equalizer and the red graph represents the desired PRBS pattern. From the figure above, it can be seen that there was a slight improvement for PRBS pattern with equalizer compared to PRBS pattern without equalizer. Even though the difference between the desired PRBS pattern and PRBS pattern with equalizer still can be seen, but there was still improvement made on the signal.
4.6  Eye Diagram

Eye diagram works as an indicator of the signal quality in high-speed digital transmissions.

4.6.1 1 Inch

Table 4.1: Comparison of eye diagrams for 1 inch
4.6.2 20 Inches

- Desired Eye Diagram

- Eye Diagram without Equalizer

- Eye Diagram with Equalizer

Table 4.2: Comparison of eye diagrams for 20 inches
Table 4.1 and Table 4.2 show the comparison of the eye diagram of microstrip with a length of 1 inch and 20 inches respectively. Based on Table 4.1, three eye diagrams were being compared. The first one was the desired eye diagram, the second one was the eye diagram without equalizer and the third one was the eye diagram with equalizer. It can be seen that the eye diagram with equalizer is almost as identical as the desired eye diagram. The difference would be on the eye diagram’s eye-opening factor. For the desired eye diagram, the value was 0.990 while for the eye diagram without equalizer the value was 0.558. For improved eye diagram, the value was 0.973 and it was not far from the value of the desired eye diagram. For eye diagram’s jitter, the value for the improved eye diagram also closed to the desired eye diagram.

For Table 4.2, three eye diagrams were being compared. It was the same as in Table 4.1 but the difference is Table 4.2 is for microstrip with a length of 20 inches. It can be seen that the eye diagram with equalizer has improved compared to the eye diagram without equalizer. The difference would be on the eye diagram’s eye-opening factor. For the eye diagram with equalizer, the value was 0.784 while for the eye diagram without equalizer the value was 0.611. For the desired eye diagram, the value was 0.825 and it had the difference of only 0.014 to the eye diagram with equalizer. For the eye diagram’s jitter, there is a significant difference between the eye diagram with equalizer to eye diagram without equalizer.
4.7 Different Configuration

The different configuration is analyzed to see whether the coefficient for different length and different termination can be used to treat the PRBS pattern of different length and different configuration respectively.

4.7.1 Same Coefficient for Different Length

In this case, the coefficient for microstrip with a length of 1 inch is used to treat the PRBS pattern for microstrip with a length of 20 inches.

![Figure 4.13: Comparison of PRBS pattern with different coefficient](image)

Figure 4.13 shows the different result of the PRBS pattern when treated with a different coefficient. The red graph shows the PRBS pattern without equalizer, the blue graph shows the PRBS pattern with equalizer used for 1 inch and the green graph shows the PRBS pattern with equalizer used for 20 inches. Based on the figure above, it can be seen that the PRBS pattern that used the equalizer for 20 inches had better improvement compared to the PRBS pattern that used the equalizer for 1 inch. Even though there was a slight improvement of using equalizer for 1 inch, it made no huge difference to the PRBS pattern without the equalizer. This shows that to improve the PRBS pattern, it is better to use the coefficients of the same length of microstrip.
4.7.2 Same Coefficient for Different Termination

For this section, the coefficient for microstrip with the termination of 120 ohms is used to treat the PRBS pattern for microstrip with the termination of 30 ohms and 70 ohms. The coefficient for microstrip with the termination of 120 ohms (length of 1 inch) is used on the PRBS pattern for microstrip with the termination of 30 ohms (length 1 inch) and 70 ohms (length of 1 inch).

Figure 4.14: Comparison of PRBS pattern with equalizer and without equalizer for termination of 30 ohms (length 1 inch)

Figure 4.15: Comparison of PRBS pattern with equalizer and without equalizer for termination of 70 ohms (length 1 inch)
Figure 4.14 and Figure 4.15 show the comparison of PRBS pattern with equalizer and without equalizer for termination of 30 ohms (length 1 inch) and termination of 70 ohms (length 1 inch) respectively. From Figure 4.14, the PRBS pattern with equalizer did not show much improvement compared to the PRBS pattern without the equalizer. This means that the coefficient used is not suitable for the termination of 30 ohms. However, for Figure 4.15 there is an improvement in the PRBS pattern with equalizer. This shows that the coefficient of 120 ohms termination can be used to repair the PRBS pattern of 70 ohms termination with length of 1 inch.

For this part, the coefficient for microstrip with the termination of 120 ohms (length of 20 inches) is used on the PRBS pattern for microstrip with the termination of 30 ohms (length 20 inches) and 70 ohms (length of 20 inches).

Figure 4.16: Comparison of PRBS pattern with equalizer and without equalizer for termination of 30 ohms (length 20 inches)
Figure 4.17: Comparison of PRBS pattern with equalizer and without equalizer for termination of 70 ohms (length 20 inches)

Figure 4.16 and Figure 4.17 show the comparison of PRBS pattern with equalizer and without equalizer for termination of 30 ohms (length 20 inches) and termination of 70 ohms (length 20 inches) respectively. From Figure 4.16, the PRBS pattern with equalizer did not show much improvement compared to the PRBS pattern without the equalizer. This means that the coefficient used is not suitable for the termination of 30 ohms. However, for Figure 4.17 there is an improvement on the PRBS pattern with equalizer. This shows that the coefficient of 120 ohms termination can be used to repair the PRBS pattern of 70 ohms termination with length of 20 inches.
Table 4.3 shows the compatibility of coefficients for different configurations and also the value of eye height and eye width for every PRBS pattern after correction. Based on the table above, it can be concluded that the coefficient for termination of 120 ohms (length 1 inch) is suitable only to termination of 70 ohms (length 1 inch) and the termination of 120 ohms (length 20 inches) is suitable only to termination of 70 ohms (length 20 inches). The coefficient is not suitable for termination of 30 ohms. This can be proved by value of eye height and the eye width. For the eye height and eye width values, only the termination of 70 ohms (1 inch and 20 inches) is almost the same with the eye height and eye width values for termination of 120 ohms after improvement. The eye height and eye width value for termination of 30 ohms (1 inch and 20 inches) are too small and differ from the value for termination of 120 ohms after improvement.

4.8 Summary

Based on all the results acquired, zero forcing equalizer had been successfully designed. It started with improving the one pulse response that has post-cursor ISI to test it on the PRBS pattern. Then, eye diagrams were generated to see the improvement of the signal quality. The coefficient for the worst case termination is also tested on different length and termination.
CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

As a conclusion, this project of zero forcing equalizer design for signal integrity application is considered as successful as both of the objectives have been achieved. The first objective was to design an equalizer with data rate of 10 Giga-bit per second using zero-forcing technique. In order to achieve this objective, one pulse response was analyzed in order to identify the post-cursor ISI. After the post-cursor ISI has been identified, desired one pulse response is used as a reference to get the coefficient to cancel the post-cursor ISI using the calculation of zero forcing. After the post-cursor ISI has been cancelled, the coefficient’s value is used on the PRBS pattern. PRBS pattern is used to test the ability of the zero forcing equalizer to mitigate the post-cursor ISI. It is also used to generate the eye diagram. The eye diagram is generated to see whether there was an improvement on the PRBS pattern after equalization. The second objective was to recommend the best equalizer setting for a different configuration. For this part, the coefficient of microstrip with a length of 1 inch is used on PRBS pattern for microstrip with a length of 20 inches to see whether it was suitable or not. It can be finalized that using the coefficient of different microstrip length on the different PRBS pattern was not suitable. It did give slight improvement but, it will be better to use its own coefficient or equalizer. Then, the coefficient is also used on different termination but with the same length. The coefficient for termination of 120 ohms is used on the termination of 70 ohms and 30 ohms to see whether it can helped to improve the PRBS pattern. After the analysis, it was found that the coefficient was only suitable to termination of 70 ohms. The coefficient cannot be used to improve the PRBS pattern for termination of 30 ohms. Therefore, for this project, there are limitations as to what the designed equalizer can achieve. There are still plenty of rooms for improvements to be made in the future.
5.2 Future Work

Equalizer design is a vast field that can be further studied and a lot of research can be done. Since this project covers the simulation of the equalizer design, further work such as fabricating the microstrip or equalizer can be carried out. Other than that, this project used the single-ended signaling but in the future, differential signaling can be used as it has better resistance to electromagnetic interference. Next, the data rate used can be higher than 10 Giga-bit per second in order to suit with the current evolving technologies. Other than that, the setting for equalizer can be improved in order to able to cater to different configurations and perhaps able to cancel both precursor and post-cursor ISI at once.
REFERENCES


[26] Seung-Woo Lee, In-Ki Hwang, Hun-Sik Kang, "Data Alignment for Multi-Channel High-Speed Interfaces using PRBS Pattern," in International Conference on Advanced Communications Technology (ICACT), Daejeon, South Korea, February 2018.


